ASMMC.036AUS

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	SOPHIE ET AL.	) Group Art Unit 2813
App. No.	:	09/975,466	)
Filed	:	October 9, 2001	)
For	:	IN SITU REDUCTION OF COPPER OXIDE PRIOR TO SILICON CARBIDE DEPOSITION	)
Examiner	:	Kielin, E.	)

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INFORMATION DISCLOSURE STATEMENT

United States Patent and Trademark Office
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Arlington, VA 22202

Dear Sir:

Enclosed is form PTO-1449 listing 11 references that are also enclosed. Applicants believe no fee is due because these references were originally cited in an Information Disclosure Statement that was filed before the receipt of a first Office Action on the merits (37 C.F.R. § 1.97(b)(3)). However, if a fee is due, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Applicants are unable to provide a date of publication for reference publication numbers 1 (SOI Technology, IBM's Next Advance in Chip Design) and 7 (slides from Sundani et al. "Oral Presentation of Dual Damascene Process"). For the purposes of examination, the Examiner is requested to assume that these publications predate the filing of the present application by more than one year.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: January 10, 2003

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ASMMC.036AUS	APPLICATION NO. 09/975,466
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)	APPLICANT SOPHIE et al.	
	FILING DATE October 9, 2001	GROUP 2812

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
	1.	SOI Technology: IBM's Next Advance In Chip Design. Date unknown.
	2.	Fukuzumi, Y. et al., "Liner-Supported Cylinder (LSC) Technology to realize Ru/Ta_2O_5/Ru Capacitor for Future DRAMs," IEEE, IED 2000, Session 34 (2000).
	3.	Hones, P. et al., "MOCVD of ThinRuthenium Oxide Films: Properties and Growth Kinetics," Chem. Vap. Deposition, Vol. 6, No. 4, pp. 193-198 (2000).
	4.	Inoue, N. et al., "Low thermal-budget fabrication of sputtered-PZT capacitor on multilevel interconnects for embedded FeRAM," IEEE, IED 2000, Session 34 (2000).
	5.	Jung, D. et al., "A Novel Ir/IrO_2/Pt-PZT-Pt/IrO_2/Ir Capacitor for A Highly Reliable Mega-Scale FRAM," IEEE, IED 2000, Session 34, (2000).
	6.	Solanki R. et al., "Atomic Layer Deposition of Copper Seed Layers," Electrochemical and Solid-State Letters, Vol. 3, No. 10, pp. 479-480 (2000).
	7.	Sundani et al., "Oral presentation of dual damascene process, slides.
	8.	Utriainen, M. et al., "Studies of metallic thin film growth in an atomic layer epitaxy reactor using M(acac)$_2$ (M = Ni, Cu, Pt) precursors," Applied Surface Science, Vol. 157, pp. 151-158 (2000).
	9.	Won, Seok-Jun et al., "Conformal CVD-Ruthenium Process for MIM Capacitor in Giga-bit DRAMs," IEEE, IED 2000, Session 34 (2000).
	10.	Xu, P. et al., "A Breakthrough in Low-k Barrier/Etch Stop Films for Copper Damascene Applications," Semiconductor Fabtech, 11th Edition, p. 239 (2000).
	11.	Yoon, Dong-Soo et al., "Investigation of RuO_2-Incorporated Pt Layer as a Bottom Electrode and Diffusion Barrier for High Epsilon Capacitor Applications," Electrochemical and Solid-State Letters, Vol. 3, No. 8, pp. 373-376 (2000).

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EXAMINER	DATE CONSIDERED

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